REMARKS

Claims 25-56 are pending. By this Amendment, claims 25, 26, 32, 37, 39 and 43-46 are amended and claims 47-56 are added. Reconsideration based on the above amendments and following remarks is respectfully requested.

I. CLAIMS 25, 27-43, 45 AND 46 SATISFIES THE REQUIREMENTS OF 35 U.S.C. §112, FIRST PARAGRAPH

The Office Action rejects claims 25, 37-43, 45 and 46 under 35 U.S.C. §112, first paragraph as containing subject matter not described in the specification. Applicants respectfully disagree with this assertion.

With respect to claim 25, the Applicants directs the Examiner to Figure 2 and pages 10-12 of the specification which disclose the gate electrode 15 having an extension 152 extending over the channel region 17.

Additionally, the Office Action asserts that this specification does not described a gate electrode comprising extensions extending outwardly above the source-drain region and further comprising extensions extending outwardly from both ends of the gate electrode. The Applicants respectfully direct the Examiner to Figure 1 which shows the gate electrode 15 having extension 151 extending from both ends of the gate electrode. Further, Figure 2 shows the gate electrode having extensions extending outwardly above the source-drain region 12. Thus, the features of claim 27 are shown in Figures 1-3.

Further, the Office Action asserts that the specification does not describe a transistor comprising a channel region with an outwardly extending extension and a gate electrode comprising extensions extending outwardly from both ends of the gate electrode. Applicants respectfully direct the Examiner to Figure 3 and page 12, line 18 of the specification which discloses a channel region having outwardly extending extension 171.

Additionally, the Office Action asserts that this specification does not describe the gate wiring layer connected to the gate electrode extensions extending outwardly above the

source-drain region by a plurality of contact holes. Applicants respectfully direct the Examiner to Figure 5 and page 15 of the specification which clearly discloses the above recited features. Finally, the Office Action asserts that the specification does not describe a gate electrode comprising extensions extending outwardly above the source-drain region wherein the extensions extend in a direction substantially perpendicular to the longitudinal direction. Applicants believe the Examiner is misinterpreting the recited claims feature. The gate electrode extensions of claim 37 are perpendicular to the longitudinal direction of the gate electrode.

Withdrawal of the rejection under 35 U.S.C. §112, first paragraph is respectfully requested.

II. CLAIMS 25-46 SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, SECOND PARAGRAPH

The Office Action rejects claims 25-46 under 35 U.S.C. §112, second paragraph as indefinite. Claims 25, 26, 32, 37, 39 and 43-46 are amended to obviate the rejection. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

III. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claims 25, 27, 28, 30, 31 and 37 under 35 U.S.C. §102(e) as anticipated by or in the alternative under 35 U.S.C. §103(a) as obvious over (U.S. Patent No. 5,821,575) to Mistry et al.; claim 44 is rejected under 35 U.S.C. §102(e) or under 35 U.S.C. §103(a) as obvious over (U.S. Patent No. 5,623,155) to Koyama; claims 26, 28, 30, 31 and 37 are rejected under 35 U.S.C. §102(e) or 35 U.S.C. §103(a) as obvious over (U.S. Patent No. 5,623,155) to Kerber et al. These rejections are respectfully traversed.

Mistry does not disclose the features of claim 27. Specifically, Mistry does not disclose a gate wiring layer electrically connected to said gate electrode and an extension of the gate electrode extending outwardly above the channel region, as claimed in claim 25.

Instead, Figure 1C of Mistry appears to disclose a gate electrode located above a source-drain region. However, there is no description of Figure 1C, nor has the Examiner cited a particular disclosure in Mistry, which shows a channel region and where the channel region is located. Thus, Mistry does not disclose an extension of the gate electrode extending outwardly above the channel region as specifically recited in claim 25.

Koyama does not disclose an extension extending outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part having two contact holes with which another contact hole is aligned, as claimed in claim 44.

Instead, Koyama teaches making one channel link shorter than another channel link which can reduce the threshold voltage required in a thin film transistor (TFT). There is no disclosure, teaching or suggestion in Koyama of the claimed features of claim 44.

Kerber does not teach, disclose or suggest the channel region including an outwardly extending extension as claimed in claim 26 and shown in Figure 3.

Instead, Kerber teaches in col. 1, line 64- col. 2, line 1 that one end of the ridge does not project beyond, or only slightly project beyond the channel region. Undesirably additional capacitances between gate electrode and the source and drain regions are thus kept optimally small. Thus, Kerber teaches away from the features of claim 26.

The applied art does not disclose the features of the claims recited above, and thus, the applied art cannot provide the advantages of the claimed invention. The fact that the applied art is devoid of the advantages shows, that it would not be obvious to one of ordinary skill in the art to modify its disclosure to make up for the deficiencies discussed above. Specifically, if it had been obvious to one of ordinary skill in the art to modify the applied art to make up for the deficiencies discussed above, then one of ordinary skill in the art would have done so to attain the advantages. However, no such disclosures have been found that shows the claimed invention.

Accordingly, withdrawal of the rejections under 35 U.S.C. §102(e) and §103(a) of claims 25, 26 and 44 is respectfully requested. Likewise, withdrawal of the rejections of the

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dependent claims which depend from the independent claims discussed above, is respectfully requested for the additional features they recite.

IV. CONCLUSION

In view of the foregoing remarks, Applicants respectfully submit that claims 25-56 define patentable subject matter and that the application is in condition for allowance.

Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:KMM/sdk

Attachment:

Appendix

Date: November 30, 2001

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320 Telephone: (703) 836-6400 DEPOSIT ACCOUNT USE
AUTHORIZATION
Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461

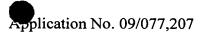


Changes to Claims:

Claims 47-56 are added.

The following are marked-up versions of the amended claims:

- 25. (Amended) A thin film transistor including a plurality of component parts comprising:
 - a channel region;
 - a gate electrode opposed to the channel region;
- a gate insulating film provided between the channel region and the gate electrode;
 - a source-drain region connected to said channel region;
 - a source-drain wiring layer electrically connected to said source-drain region;
 - a gate wiring layer electrically connected to said gate electrode,
- an extension of the gate electrode extending outwardly provided above the channel region-being formed.
- 26. (Amended) The thin film transistor including a plurality of component parts comprising:
 - a channel region;
 - a gate electrode opposed to the channel region;
- a gate insulating film provided between the channel region and the gate electrode;
 - a source-drain region connected to said channel region;
 - a source-drain wiring layer electrically connected to said source-drain region;
 - a gate wiring layer electrically connected to said gate electrode,



an extension of wherein the channel region includes an outwardly extending outwardly therefrom being formed extension.

- 32. (Amended) The thin film transistor according to Claim 25, an extension of wherein the channel region includes an outwardly extending outwardly therefrom being formed extension.
- 37. (Amended) The thin film transistor according to Claim 25 or 26, the formed extension extending in a direction substantially perpendicular to the a longitudinal direction.
- 39. (Amended) The display device according to Claim 38, the formed extension extending in a direction substantially perpendicular to the a longitudinal direction.
- 43. (Amended) A liquid crystal display device according to Claim 38, the formed extension extending in a direction substantially perpendicular to the a longitudinal direction.
- 44. (Amended) A thin film transistor including a plurality of component parts comprising:
 - a channel region;
 - a gate electrode opposed to the channel region;
- a gate insulating film provided between the channel region and the gate electrode;
 - a source-drain region connected to said channel region;
 - a source-drain wiring layer electrically connected to said source-drain region;
 - a gate wiring layer electrically connected to said gate electrode,
- comprising a extension extending outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part being defined by having two contact holes with which another contact hole is aligned.
- 45. (Amended) The thin film transistor according to claim 44, an extension of the gate electrode extending outwardly provided above the channel being formed region.

46. (Amended) The thin film transistor according to claim 44, anextension wherein of the channel region includes an outwardly extending outwardly therefrom being formed extension.